IME-03-005

March 5, 2004

Commissioner for Patents P.O.Box 1450 Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572 28 Davis Avenue Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/748,736 12/30/03

Wong Ee Hua et al.

WAFER LEVEL SUPER STRETCH SOLDER

## INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

## CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March ) 6, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 53 16 04

- U.S. Patent 5,251,806 to Agarwala et al., "Method of Forming Dual Height Solder Interconnections," discloses an interconnection and a method for making the same.
- U.S. Patent 5,441,195 to Tustaniwskyj et al., "Method of Stretching Solder Joints," discusses a method of stretching solder joints between the input/ouput pads of an electrical component and corresponding input/output pads on a substrate.
- U.S. Patent 5,964,396 to Brofman et al., "Enhanced Ceramic Ball Grid Array Using In-Situ Solder Stretch with Clip," discloses a device for stretching solder interconnection joints between two substrates of an electronic module.
- U.S. Patent 5,975,409 to Brofman et al., "Ceramic Ball Grid Array Using In-Situ Solder Stretch," discloses a method and apparatus for forming an elongated solder joint between two soldered substrates of an electronic module by applying a controlled separating force between the two soldered substrates during and/or after heating of the module.
- U.S. Patent 6,442,831 to Khandros et al., "Method for Shaping Spring Elements," discusses free-standing bond wires used as core elements for composite interconnection element.

IME-03-005

U.S. Patent 5,790,377 to Schreiber et al., "Integral Copper Column with Solder Bump Flip Chip," discloses an integral copper column with a solder bump flip chip.

Larry Gilg, Die Products Consortium, Austin, TX-EP&P, 7/1/02, "Wafer-Level vs. Singulated Die Burn-In and Test," discusses IC manufacturers that supply die products developing several powerful tools to provide the reliability demanded by today's high performance ICs.

Beth Keser et al., "Encapsulated Double-Bump WL-CSP:

Design and Reliability," Proc. 51st Electronic Component Tech.

Conf. 2001, pp. 35-39, discusses a new type of wafer level

package designed and fabricated by using an encapsulation

material which is applied directly to a bumped wafer.

J. Simon, "Development and Board Level Reliability of a Wafer-level CSP," Proc. 41st IEMT/IMC 2000, pp. 22-27, discusses the requirements and limitations for waferlevel CSP manufacturing.

In the publication, S.I. Denda, et al., "Wafer Level Packaging Technology in Japan," Proc. 4th IEMT/IMC, 2000, pp. 4-9, (Fig. 2), an overview of WLP technology in Japan is made, and their categorization and possible technical problems are discussed.

IME-03-005

Advanced IC Packaging Markets and Trends, pp. 4-49 to 4-51, Electronic Trend Publication, 6th Edition, 2002, provides innovative and integrated flip chip solutions to companies that manufacture semiconductors.

Bakir, et al., "Sea of Leads Ultra High-Density Compliant Wafer-Level Packaging Technology," Proc. 52nd Elec. Component Tech. Conf., 2002, pp. 1087-1094, discusses Sea of Leads (SoL), a novel ultra high-density compliant wafer-level packaging technology.

P. Garrou, et al., "Cyclotene BCB Resin for Bumping and Wafer Level Chip Scale Packaging (WL-CSP), Proc. 3rd IEMT/IMC, pp. 206-211, 1999, discusses wafer level CSP (WL-CSP) appearing to be a strong candidate for low cost CSP technolog of the future.

Sincerely,

Stephen B. Ackerman,

Reg. No. 37761

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